## G99/1-3 Type Test Verification Report

Inverter Mode	I				ATG-5K-TL		
Manufacturer	Reference n	umber					
Micro-generate	or technolog	ÿ		F	lybrid inverter		
Manufacturer	name			Aton	Green Storage SpA		
Registered offi	ce address		Via	Nuova Circonvallaz	ione, 57/B - 47923 Rimini (RN), Italy		
Operational he	adquarters	address		Via Guido Rossa, 5	– 41057 Spilamberto (MO), Italy		
Tel	+3959783	3939		Tel	+3959783939		
E:mail	a.ferrero	@atonstorag	e.com	E:mail	a.ferrero@atonstorage.com		
				Connection Option			
Maximum rate	d capacity	5		kW single phase			
Tested referen	ce number w or to shipmer	vill be manufa nt to site and t	ctured an	d tested to ensure t	ed by the company with the above Type hat they perform as stated in this required to ensure that the product		
Signed	Mr. Ettore Uguzzoni		oni	On behalf of	Aton Green Storage SpA		
- the internal lal and with the Ma New District, Jia - or at external l	ooratories of anufacturer's ngsu, PRC; aboratories i	the Company to brand: Jiangsu dentified by Jia	that produ I GoodWe angsu Goo		Inder Test on behalf of the Manufacturer ology Co., Ltd No. 90 Zijin Road, Suzhou rechnology Co., Ltd.		



**1. Operating Range:** Two tests should be carried with the Power Generating Module operating at Registered Capacity and connected to a suitable test supply or grid simulation set. The power supplied by the primary source shall be kept stable within  $\pm 5$  % of the apparent power value set for the entire duration of each test sequence.

Frequency, voltage and Active Power measurements at the output terminals of the Power Generating Module shall be recorded every second. The tests will verify that the Power Generating Module can operate within the required ranges for the specified period of time.

The Interface Protection shall be disabled during the tests.

In case of a PV Power Park Module the PV primary source may be replaced by a DC source.

In case of a full converter Power Park Module (eg wind) the primary source and the prime mover Inverter/rectifier may be replaced by a DC source.

Test 1	
Voltage = 85% of nominal (195.5 V)	Result
Frequency = 47 Hz	Pass
Power factor = 1	Pass
Period of test 20s	
Test 2	
Voltage = 85% of nominal (195.5 V)	Result
Frequency = 47.5 Hz	Pass
Power factor = 1	Pass
Period of test 90 minutes	
Test 3	
Voltage = 110% of nominal (253 V).	Result
Frequency = 51.5 Hz	Pass
Power factor = 1	Fass
Period of test 90 minutes	
Test 4	
Voltage = 110% of nominal (253 V).	Result
Frequency = 52.0 Hz	Pass
Power factor = 1	Fass
Period of test 15 minutes	



2. Power Qualit	y – Harmonics:						
For Power Gene	(ie 50 kW) the						
test requiremer	its are specified in	n Annex A.7.1.5.	These tests should	be carried out	as specified in		
BS EN 61000-3-	12 The results ne	ed to comply wi	th the limits of Ta	ble 2 of BS EN 6	51000-3-12 for		
single phase equ	uipment and Table	e 3 of BS EN 6100	00-3-12 for three	phase equipmen	t.		
• •	•		o the limits laid d			Pass	
	-		2 and 4 times the		-		
Module in order	r to accept the cor	nection to a Dist	ribution Network.	-	-		
For Power Gene	erating Modules o	of Registered Cap	acity of greater th	an 75 A per ph	ase (ie 50 kW)		
the installation	must be designed	in accordance wi	th EREC G5.				
Power Generati	ng Module tested	to BS EN 61000-3	3-12				
Micro-gen	erator rating per p	hase (rpp)	kv	Ά	Harmonic % =	Measured Value	
						per phase (kVA)	
	Сара	acity					
Harmonic	Measured	%	Measured	%	1 phase	3 phase	
	Value (MV) in		Value (MV) in				
	Amps		Amps				
2nd	0.162	0.81%	0.317	1.59%	8%	8%	
3rd	0.089	0.45%	0.089	0.45%	21.6%	Not stated	
4th	0.016	0.08%	0.027	0.14%	4%	4%	
5th	0.064	0.32%	0.075	0.38%	10.7%	10.7%	
6th	0.019	0.10%	0.022	0.11%	2.67%	2.67%	
7th	0.066	0.33%	0.066	0.33%	7.2%	7.2%	
8th	0.010	0.05%	0.007	0.04%	2%	2%	
9th	0.049	0.25%	0.051	0.26%	3.8%	Not stated	
10th	0.008	0.04%	0.010	0.05%	1.6%	1.6%	
11th	0.045	0.23%	0.044	0.22%	3.1%	3.1%	
12th	0.012	0.06%	0.015	0.08%	1.33%	1.33%	
13th	0.033	0.17%	0.036	0.18%	2%	2%	
THD12	0.221	1.11%	0.355	1.77%	23%	13%	
PWHD13	0.438	2.19%	0.596	2.98%	23%	22%	



3. Power Quality – Voltage fluctuations and Flicker:				
For Power Generating Modules of Registered Capacity of less than 75 A per phase (ie 50 kW) these				
tests should be undertaken in accordance with Annex A.7.1.4.3. Results should be normalised to a				
standard source impedance, or if this results in figures above the limits set in BS EN 61000-3-11 to a				
suitable Maximum Impedance.				
For Power Generating Modules of Registered Capacity of greater than 75 A per phase (ie 50 kW) the				
installation must be designed in accordance with EREC P28.				

	Starting			Stopping			Running	
	d <sub>max</sub>	d <sub>c</sub>	d <sub>(t)</sub>	d <sub>max</sub>	dc	d <sub>(t)</sub>	Pst	Plt 2 hours
Measured Values at test	0.44	0.04	0	0.48	0.05	0	0.19	0.17
impedance	0.44	0.04	0	0.40	0.05	0	0.19	0.17
Normalised to standard	0.352	0.032	0	0.384	0.04	0	0.152	0.136
impedance	0.332	0.032	0	0.564	0.04	0	0.152	0.150
Limits set under BS EN	10/	3.3%	3.3%	4%	3.3%	3.3%	1.0	6.5
61000-3-2	4%	5.570	5.5%	470	5.5%	5.5%	1.0	0.5

Applies to three phase and split single phase Micro-generators.

^ Applies to single phase Micro-generators and Micro-generators using two phases on a three phase system.

For voltage change and flicker measurements the following formula is to be used to convert the measured values to the normalized values where the power factor of the generation output is 0.98 or above.

Normalized value = Measured value × reference source resistance/measured source resistance at test point × 3.68/rating per phase.

Single phase units reference source resistance is 0.4  $\Omega$ 

Two phase units in a three phase system reference source resistance is 0.4  $\Omega$ .

Two phase units in a split phase system reference source resistance is 0.24  $\Omega$ .

Three phase units reference source resistance is  $0.24 \Omega$ .

Where the power factor of the output is under 0.98 then the X to R ratio of the test impedance should be close to that of the Standard Impedance.

The stopping test should be a trip from full load operation.

The duration of these tests need to conform to the particular requirements set out in the testing notes for the technology under test. Dates and location of the test need to be noted below.

4. Power quality. DC injection	Pass		
This test should be carried out	PdSS		
Test level power	10%	55%	100%
Recorded value in Amps	0.0025	0.0016	0.004
As % of rated AC current	0.0125%	0.008%	0.020%
Limit	0.25%	0.25%	0.25%



5. Power Quality. Power fact	or		
This test shall be carried out i	n accordance with EN 50538 An	nex D.3.4.1 but with nominal vo	oltage Pass
-6% and +10%. Voltage to be	maintained within ±1.5% of the	stated level during the test.	
	216.2 V	230 V	253 V
20% of Registered Capacity	0.9644	0.9580	0.9785
50% of Registered Capacity	0.9964	0.9956	0.9937
75% of Registered Capacity	0.9987	0.9986	0.9980
100% of Registered	0.9990	0.9991	0.9990
Capacity	0.5550	0.5551	0.5550
Limit	>0.95	>0.95	>0.95

6. Protection. Fre		Dace				
These tests shoul		Pass				
Function	Sett	ting	Trip	test	No trip test	
	Fraguanay	Time delay	Frequency	Time delay	Frequency /	Confirm no
	Frequency	Time delay	Frequency	Time delay	time	trip
		20 -	47.40.11-	20.226	47.7Hz /	na tria
U/F stage 1	47.5 Hz	20 s	47.49 Hz	20.23s	25s	no trip
	47.11-	0.5.6	47.00.11-	0.65	47.2Hz /	no trip
U/F stage 2	47 Hz	0.5 s	47.00 Hz	0.65s	19.98s	
					46.8Hz /	na tria
					0.48s	no trip
O/E stage 1	F2 11-	0.5.4	F2 01 U-	0.646	51.8Hz /	no trin
O/F stage 1	52 Hz	0.5 s	52.01 Hz	0.64s	89.98s	no trip
					52.2Hz /	no trin
					0.48s	no trip
Note. For frequer	ncy trip tests the f	frequency require	ed to trip is the se	tting ± 0.1 Hz. In (	order to measure	the time delay

Note. For frequency trip tests the frequency required to trip is the setting  $\pm$  0.1 Hz. In order to measure the time delay a larger deviation than the minimum required to operate the projection can be used. The "No trip tests" need to be carried out at the setting  $\pm$  0.2 Hz and for the relevant times as shown in the table above to ensure that the protection will not trip in error.



Protection. Voltage test These tests should be carried out in accordance with Annex A.7.1.2.2						Pass	
Function	Set	ting	Trip	test	No tri	ip test	
	Voltage	Time delay	Voltage	Time delay	Voltage / time	Confirm no trip	
U/V stage 1	184 V	2.5 s	185.3V	2.63s	188V / 3.5s	no trip	
					180V / 2.48s	no trip	
O/V stage 1	262.2 V	1.0 s	261.9V	1.11s	258.2V 2.0s	no trip	
O/V stage 2	273.7 V	0.5 s	273.2V	0.642s	269.7V 0.98s	no trip	
					277.7V 0.48s	no trip	

deviation than the minimum required to operate the protection. The No trip tests need to be carried out at the setting  $\pm 4$  V and for the relevant times as shown in the table above to ensure that the protection will not trip in error.

8. Protection. Loss of Mains test								
These tests should be carried out in accordance with BS EN 62116. Annex A.7.1.2.4.								
The following sub se	The following sub set of tests should be recorded in the following table							
	33%	66%	100%	33%	66%	100%		
Test Power and imbalance	-5% Q	-5% Q	-5% P	+5% Q	+5% Q	+5% P		
inibalance	Test 22	Test 12	Test 5	Test 31	Test 21	Test 10		
Trip time. Limit is 0.5s	0.0868s	0.0998s	0.145s	0.110s	0.1304s	0.1512s		

Protection - Frequency change, Vector Shift Stability test: This test should be carried out in							
accordance with EREC G98	8 Annex A1 A.1.2.6 (Inverte	er connected) or Annex	A2 A.2.2.6	Pass			
(Synchronous).	(Synchronous).						
	Start Frequency Change Confirm			m no trip			
Positive Vector Shift	49Hz	+50 degrees	no trip				
Negative Vector Shift	50.5Hz	- 50degrees	n	o trip			



Protection – Frequency change, RoCoF Stability test: The requirement is specified in section 11.3,						
test procedure in Annex A.1.2	test procedure in Annex A.1.2.6 (Inverter connected) or Annex A2 A.2.2.6 (Synchronous).					
Ramp range	Test frequency ramp:	Test Duration	st Duration Confirm no trip			
49.0 Hz to 51.0 Hz	+0.95Hz/sec	2.1 s	n	o trip		
51.0 Hz to 49.0 Hz	-0.95Hz/sec	2.1 s	n	o trip		
Ramp range	Test frequency ramp:	Trip time limit	Tri	p time		
49.0 Hz to 51.0 Hz	+1Hz/sec	0.5s	0	.780s		
51.0 Hz to 49.0 Hz	-1Hz/sec	0.5s	0	.800s		

9. Limited Frequency Sensitive I	Mode – Overfrequenc	y test: This test shoul	d be carried out in	
accordance with EN 50438 Annex D.3.3 Power response to over- frequency. The test should be			Pass	
carried out using the specific thre	shold frequency of 50.	4 Hz and <b>Droop</b> of 10%	, ).	
Test sequence at Registered	Measured Active	Frequency	Primary Power	Active Power
Capacity >80%	Power Output		Source	Gradient
Step a) 50.00 Hz ±0.01 Hz	5051	50	5271	
Step b) 50.45 Hz ±0.05 Hz	4983	50.45	5203	27.20%
Step c) 50.70 Hz ±0.10 Hz	4756	50.7	4956	19.67%
Step d) 51.15 Hz ±0.05 Hz	4284	51.15	4459	20.45%
Step e) 50.70 Hz ±0.10 Hz	4757	50.7	4957	19.60%
Step f) 50.45 Hz ±0.05 Hz	5000	50.45	5217	20.40%
Step g) 50.00 Hz ±0.01 Hz	5052	50	5274	
Test sequence at Registered	Measured Active	Frequency	Primary Power	Active Power
Capacity 40% - 60%	Power Output		Source	Gradient
Step a) 50.00 Hz ±0.01 Hz	2530	50	2639	
Step b) 50.45 Hz ±0.05 Hz	2467	50.45	2576	25.20%
Step c) 50.70 Hz ±0.10 Hz	2230	50.7	2324	20.00%
Step d) 51.15 Hz ±0.05 Hz	1758	51.15	1836	20.59%
Step e) 50.70 Hz ±0.10 Hz	2227	50.7	2321	20.20%
Step f) 50.45 Hz ±0.05 Hz	2474	50.45	2584	22.40%
Step g) 50.00 Hz ±0.01 Hz	2525	50	2634	

## 10. Protection. Re-connection time

Test should prove that the reconnection sequence starts after a minimum delay of 20 s for restoration of voltage and frequency to within the stage 1 settings of Table 10.1.

Time delay setting				
Measured delay time(s)	At 258.2V	At 204.1V	At 47.6Hz	At 51.9Hz
	47s	47.4s	47.4s	46.4s
Confirmation that the SSEG	At 266.2V	At 196.1V	At 47.4Hz	At 52.1Hz
does not re-connect	no reconnection	no reconnection	no reconnection	no reconnection



Pass

<b>11. Fault level contribution</b> : These te G98 Annex A1 A.1.3.5 (Inverter connect	Pass	
	For Inverter output	
Time after fault	Volts	Amps
20ms	3.464	8.1878
100ms	6.544	-10.8917
250ms	2.849	-5.2014
500ms	-2.695	-0.8449
Time to trip	59.2ms	In seconds

12. Self-Monitoring solid state switching: No specified test requirements. Refer to Annex A.7.1.7.		
It has been verified that in the event of the solid state switching device failing to		
disconnect the Power Park Module, the voltage on the output side of the switching	N/A	
device is reduced to a value below 50 volts within 0.5 s.		

13. Wiring functional tests: If required by para 15.2.1.	
Confirm that the relevant test schedule is attached (tests to be undertaken at time of	N /A
commissioning)	N/A

14. Logic Interface (input port).	
Confirm that an input port is provided and can be used to shut down the module.	Pass

dditional comments	
IA	

